



#4/Priority
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3/12/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **Narumi OHKAWA**

Serial No.: **NEW**

Filed: **April 8, 1999**

For: **SEMICONDUCTOR DEVICE HAVING BOTH MEMORY AND LOGIC CIRCUIT
AND ITS MANUFACTURE**

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CLAIM FOR PRIORITY UNDER 35 U.S.C. 119

Assistant Commissioner for Patents
Washington, D. C. 20231

Date: April 8, 1999

Sir:

The benefit of the filing date of the following prior foreign application is hereby requested for the above-identified application, and the priority provided in 35 U.S.C. 119 is hereby claimed:

Japanese Appln. No. 10-281699, Filed October 2, 1998

In support of this claim, the requisite certified copy of said original foreign application is filed herewith.

It is requested that the file of this application be marked to indicate that the applicant has complied with the requirements of 35 U.S.C. 119 and that the Patent and Trademark Office kindly acknowledge receipt of said document.

In the event that any fees are due in connection with this paper, please charge our Deposit Account No. 01-2340.

Respectfully submitted,

**ARMSTRONG, WESTERMAN, HATTORI,
MCLELAND & NAUGHTON**

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別紙添付の書類に記載されている事項は下記の出願書類に記載されて
る事項と同一であることを証明する。

This is to certify that the annexed is a true copy of the following application as filed
in this Office.

出願年月日
Date of Application:

1998年10月 2日

出願番号
Application Number:

平成10年特許願第281699号

出願人
Applicant(s):

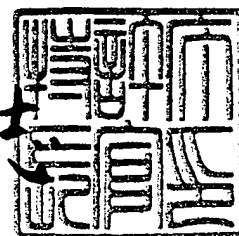
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1999年 2月19日

特許庁長官
Commissioner,
Patent Office

伴佐山 建志



出証番号 出証特平11-3008041